

正基科技股份有限公司

SPECIFICATION

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Company	
Representative Signature	

PREPARED	REVIEW			APPROVED	DCC ISSUE
	PM	QA	ET		
			PE		
			ME		
			APPROVED		



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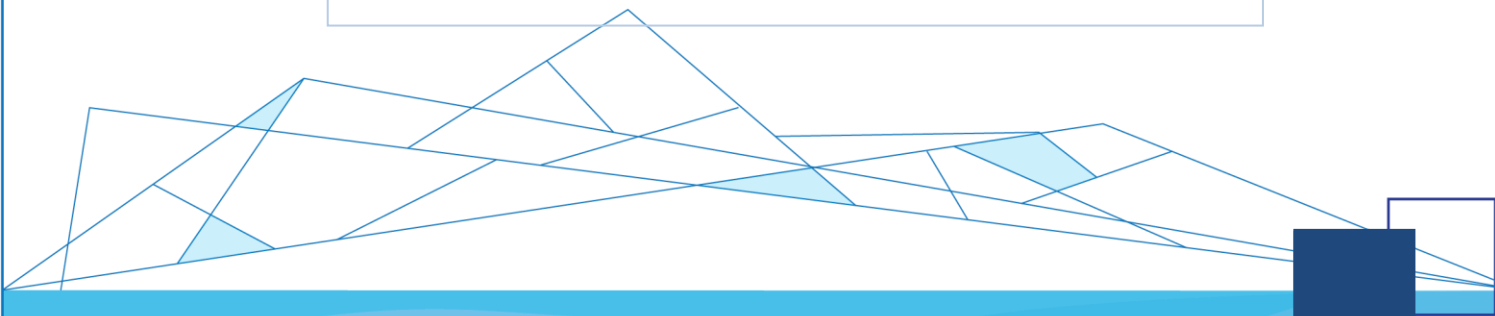
AP6208

Data Sheet

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Revision

Revision	Date	Description	Revised By
0.1	2024/10/11	-Preliminary Release	Ander Lee
0.2	2025/04/15	-Update RF Specification	Ian
0.3	2025/06/25	-Update System Block Diagram	Ian



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1. Introduction

Ampak Technology would like to release a low-cost, small size, low-power consumption module which includes BLE functionalities. The highly integrated AP6208 module makes the possibilities of Bluetooth 5.4 Low Energy, Multiprotocol dual radio, Zigbee, Thread and Matter protocols 2.4 GHz proprietary modulations multi-rate, Building automation, Medical, Industrial transport-asset tracking, Factory automation and control...etc. application.

1.1 Description

This compact module is a total solution for a combination of Dual-Radio Bluetooth 5.4 and IEEE 802.15.4 technologies with Microcontroller Processor. The module is specifically developed for embedded system devices. The AP6208 module also integrates an Arm Cortex-M4 CPU running at 160 MHz and has a high-speed UART interface for connection with an external host processor.

The BT system is a dual-radio Bluetooth 5.4+ compliant baseband processor and 2.4 GHz transceiver. It also has tightly-coupled support for IEEE 802.15.4 (Thread, Zigbee, etc.) using the 2.4 GHz Bluetooth radio.

The BT system supports all mandatory SIG BT 5.4+ features. In addition, it supports ranging technologies such as high-accuracy distance measurement (HADM), which is expected to be included in Bluetooth standards greater than BT 5.4+.

The AP6208 module also supports worldwide regulatory requirements and the latest publicly available revisions of the Thread, Zigbee, and Matter standards.

The BT system includes an Arm core (running at 160 MHz) paired with 1640 KB of ROM memory for program storage and boot ROM, 544 KB of system-data RAM, and 1664 KB of code RAM. It also has 256 bytes of user accessible OTP for storing wafer ID, RF/analog calibration settings, and other system configuration settings.

1.2 Applications

- Building automation
- Industrial transport – asset tracking
- Factory automation and control
- Medical

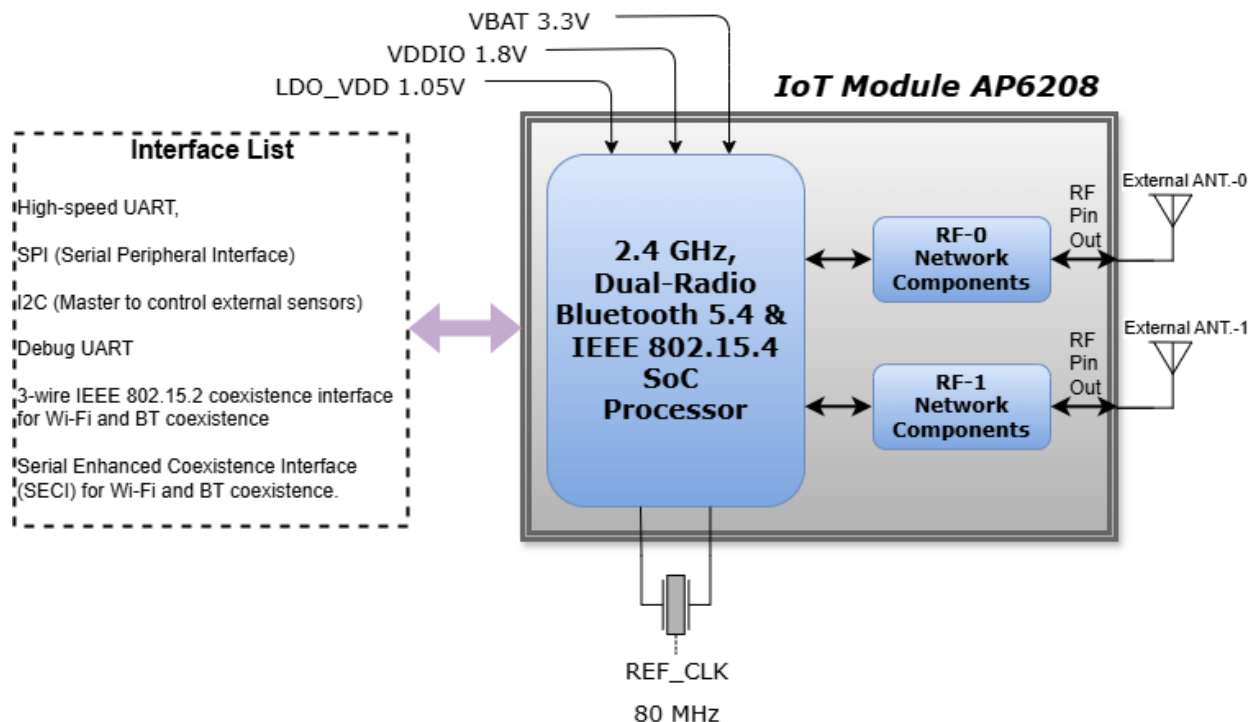


2. Features

- Complies with BT Core Specification Version 5.4 with support for future 6.0 specifications such as high accuracy distance measurement (HADM).
- Supports two 2.4 GHz band radios concurrently.
- Supports Bluetooth Class 1 and Class 2 TX operation.
- Supports Electronic Shelf Label (ESL).
- Supports HADM/channel sounding (BT 6.0 compliance expected).
- Supports BLE-LR, angle of departure (AoD), angle of arrival (AoA), and HW-capable ISOC.
- Supports BLE Zephyr open-source software stack.
- Supports IEEE 802.15.4 (OpenThread and ZBOSS) up to version 2.
- Supports firmware download over UART for shared flash with a host processor, or from local, dedicated serial flash over an SPI.
- Four GPIO and antenna-selection pins for AoD and AoA determination or HADM (channel sounding).
- Supports secure boot.

A simplified block diagram of the module is depicted in the figure below.

System Block Diagram



3. General Specification

3.1 General Specification

Model Name	AP6208
Product Description	2.4 GHz, Dual-Radio Bluetooth 5.4 and IEEE 802.15.4 Module
Dimension	L x W : 12 x 12 (typical) mm , H : 1.78 (Maximum) mm
Module type package	Stamp type with metal lid
MCU Interface	High-speed UART, SPI, I2C, Debug UART
	3-wire IEEE 802.15.2 coexistence interface for Wi-Fi and BT coexistence SECI for Wi-Fi and BT coexistence
Operating temperature	-40°C to 85°C
Storage temperature	-40°C to 105°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

3.2 DC Characteristics

3.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VDD_3P3V	DC Power supply for SIP Module 3.3V	-0.5	3.7	V
VDD_1P8V	DC Power supply for SIP Module 1.8V	-0.4	2.07	V
VDD_1P05V	DC Power supply for SIP Module 1.05V	-0.4	1.2075	V

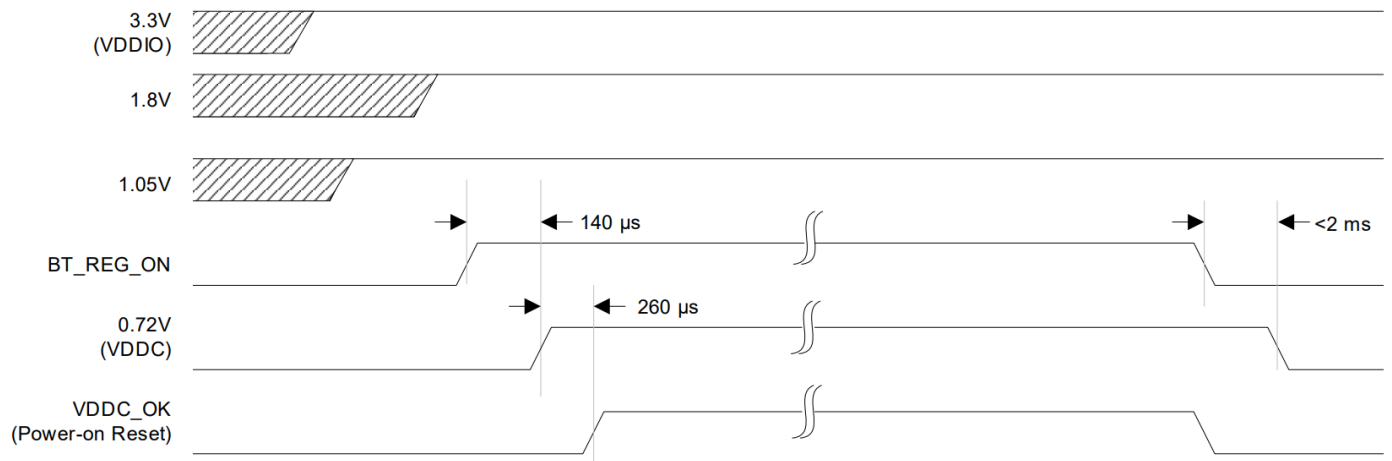
3.2.2 Recommended Operating Ratings

Symbol	Min.	Typ.	Max.	Unit
VDD_3P3V	3.135	3.3	3.456	V
VDD_1P8V	1.71	1.8	1.89	V
VDD_1P05V	1.008	1.05	1.092	V

3.3 Power Sequence

The AP6208 module is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

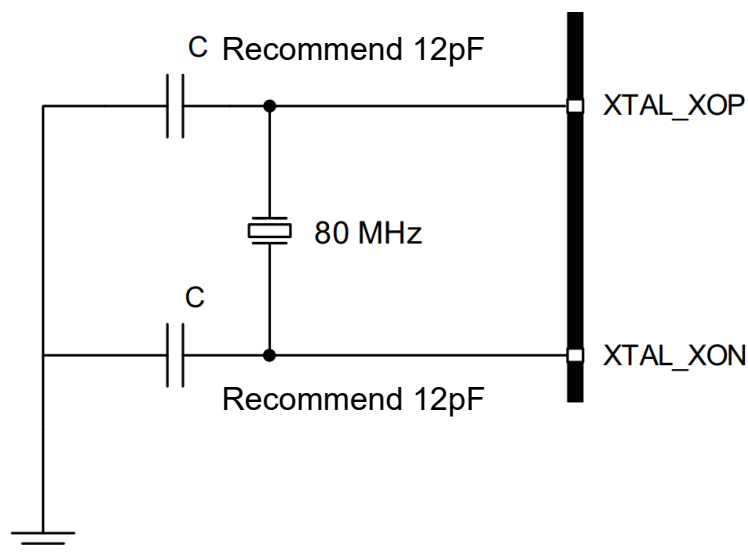
The figure below shows the power sequence diagram.



3.4 Frequency References

An external crystal is used for generating all radio frequencies and normal-operation clocking.

The AP6208 module uses an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in below figure. Consult the reference schematics for the latest configuration.



The recommended default frequency reference is an 80 MHz crystal. The signal characteristics for the crystal oscillator interface are provided in below table and Crystal oscillator requirements^a.

Parameter	Conditions/Notes	Crystal ^b			Unit
		Min.	Typical	Max.	
Frequency	—	—	80	—	MHz
Frequency tolerance over the lifetime of the equipment, including temperature ^c	Without trimming	-20	—	20	ppm
Crystal load capacitance	—	—	8	—	pF
ESR	—	—	—	50	Ω
Drive level	External crystal must be able to tolerate this drive level.	150	—	—	μW

a. The parameter values in this table apply when using an 80 MHz crystal.

b. Use BT_XTAL_XOP and BT_XTAL_XON.

c. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.

4. System Interface

4.1 UART Host Interface

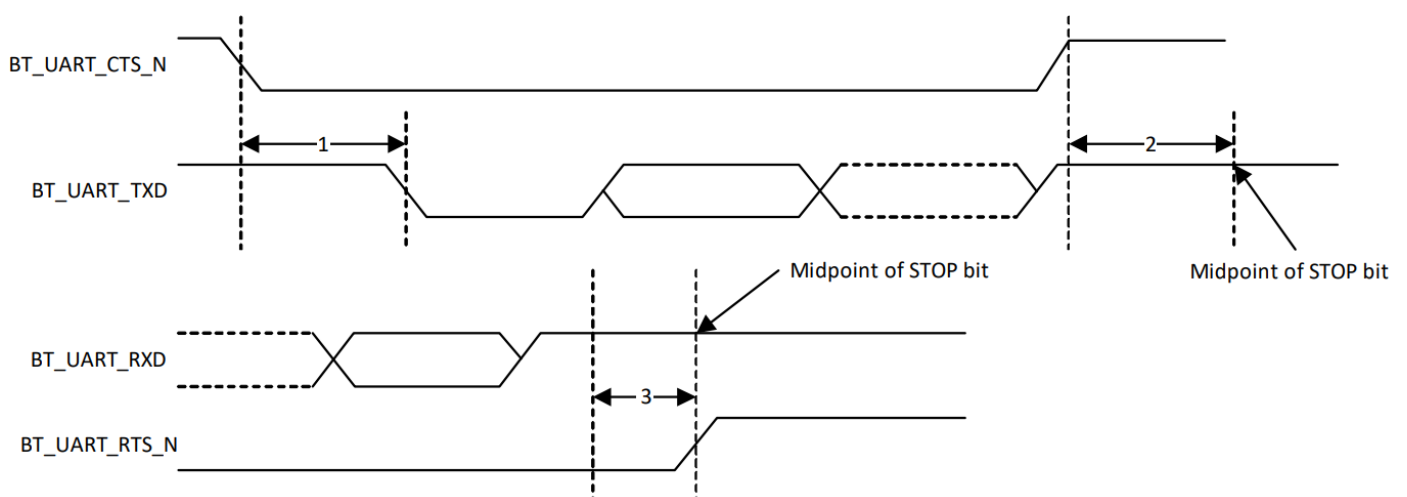
The AP6208 module UART host interface is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 12 Mbps. The baud rate may be selected through a vendor-specific UART HCI command. The UART has a 2600-byte receive FIFO and a 2600-byte transmit FIFO to support host-transport traffic. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.4 UART HCI specification: H4, a custom Extended H4, and H5, as well as the OpenThread Spinel protocol. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The AP6208 module UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AP6208 module UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within $\pm 2\%$.

The diagram below is UART timing.



UART Timing specifications:

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	—	—	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	—	—	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	—	—	0.5	Bit periods

4.2 Peripheral/Debug UART Interface

The peripheral/debug UART has the following features:

- ✧ 256-byte RX and TX FIFOs.
- ✧ A 4-pin interface.

The PUART_RXD and PUART_TXD signals can be multiplexed to one of the following three pairs of pins, respectively:

- ✧ TX_CONFX2 and BT_STATUS2

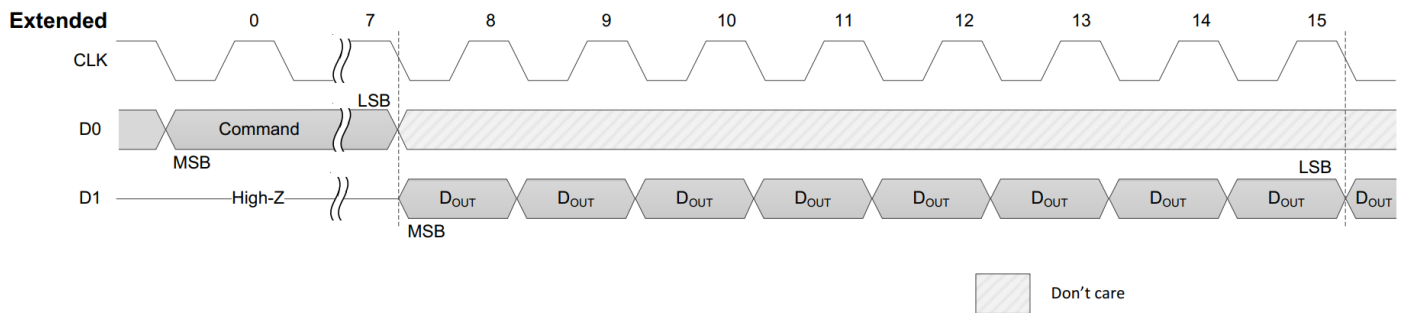
4.3 Serial Flash Interface

The serial flash interface supports the following features:

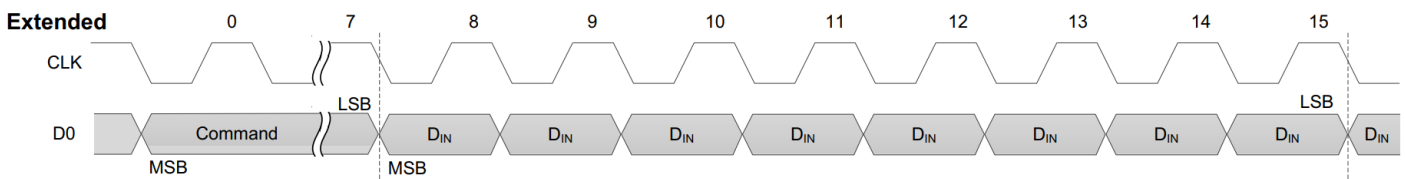
- ✧ A SPI-compatible serial bus.
- ✧ A maximum serial flash size of 64 MB.
- ✧ A 24 MHz (maximum) clock frequency.
- ✧ Support for either $\times 1$ or $\times 4$ addresses with two data lines (one input and one output).
- ✧ 3-byte and 4-byte addressing modes.
- ✧ A configurable dummy-cycle count that is programmable from 1 to 15.
- ✧ Programmable instructions output to serial flash.
- ✧ An option to change the sampling edge from rising-edge to falling-edge for read-back data when in high speed mode.

Note: To minimize ripple at the AP6208 module of SPI_CLK port to within $\pm 20\%$ of VDDIO due to transmission-line effects, use a series resistor on the SPI_CLK line to the serial flash, preferably close to the serial flash port.

Serial flash read-register timing

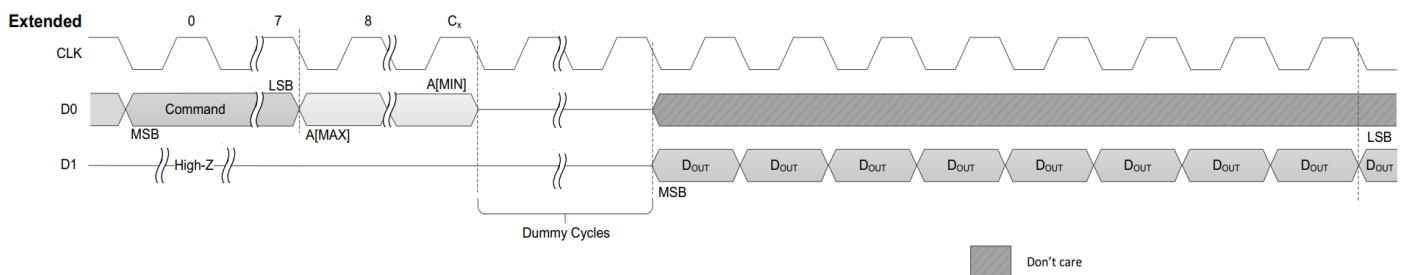


Serial flash write-register timing



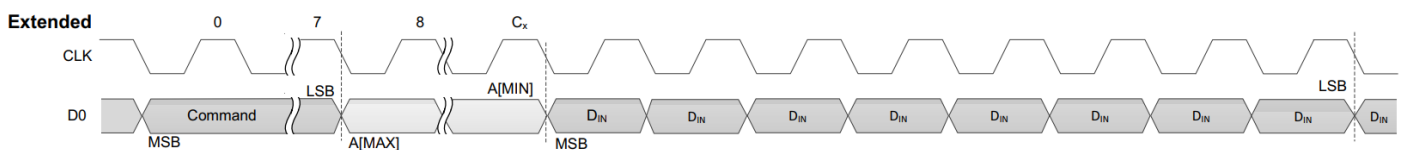
Memory fast-read timing

- ✧ 24-bit addressing is used, so A[MAX] = A[23] and A[MIN] = A[0].
- ✧ For an extended SPI protocol, $C_x = 7 + (A[\text{MAX}] + 1)$.



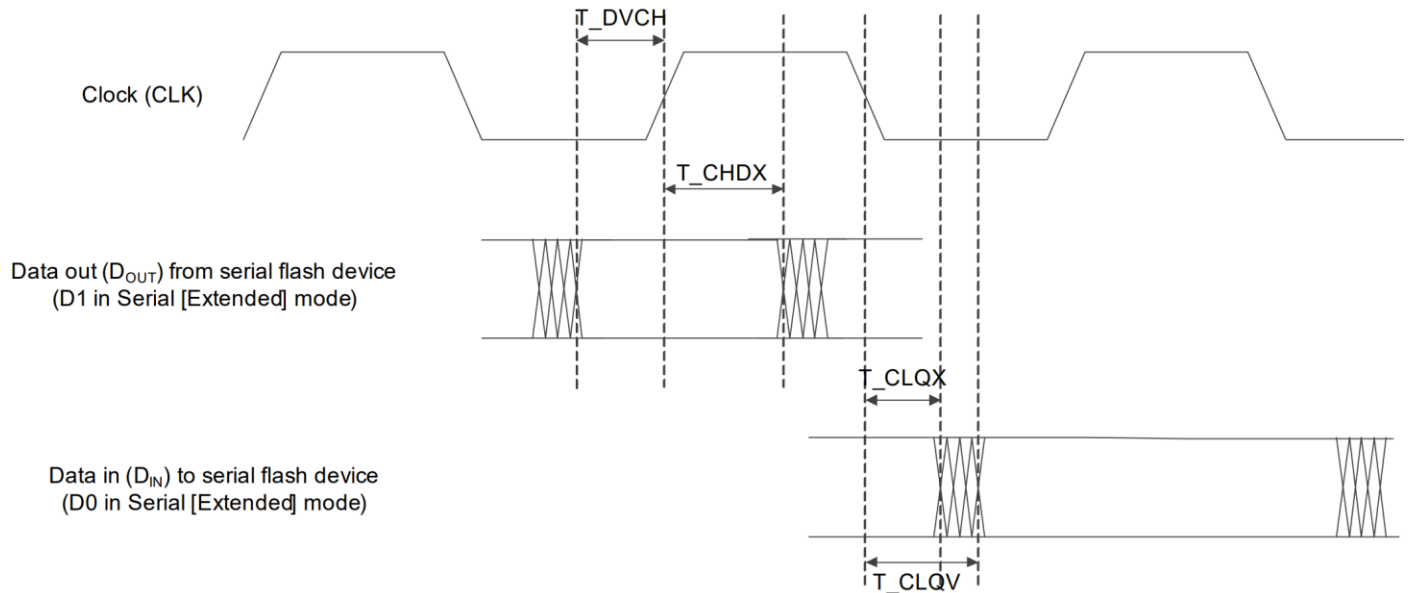
Memory-write timing

For an extended SPI protocol, $C_x = 7 + (A[\text{MAX}] + 1)$



4.4 Serial Flash Parameters

Serial flash timing parameters diagram

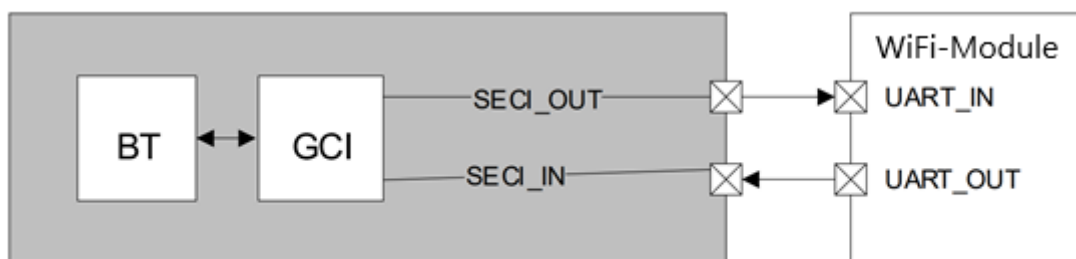


Serial flash timing parameters table

Parameter	Description	Minimum	Maximum	Unit
T_{DVCH}	Data setup time	2	–	ns
T_{CHDX}	Data hold time	3	–	ns
T_{CLQX}	Output hold time	1	–	ns
T_{CLQV}	Output valid time (with a 10 pF load)	–	5	ns

4.5 Serial Enhanced Coexistence Interface

An external handshake interface is available to enable signaling between the device and an external co-located wireless device, such as a Wi-Fi IC, to manage wireless medium sharing for optimum performance. The below figure shows the Wi-Fi coexistence interface.



NOTE: SECI_OUT and SECI_IN are multiplexed on the GPIOs.

4.6 I²C Interface

The AP6208 module supports a I2C master interface. The Standard, Fast, and Fast-mode Plus modes are supported. The I2C interface is a 2-wire serial bus that is compatible with the I2C Specification (version 2.1).

The AP6208 module I2C interface supports the following features:

- ✧ Parallel-to-I2C bus protocol converter and interface.
- ✧ Standard mode (100 kbps), Fast mode (400 kbps), and Fast-mode Plus (1 Mbps).
- ✧ Single-master capability.
- ✧ Support for both 7-bit and 10-bit addressing.
- ✧ Available as a GPIO alternate function.
- ✧ Clock and data glitch filtering.

The SCL and SDA signals can be multiplexed to one of the following four pairs of pins, respectively:

- ✧ TDO and TDI.
- ✧ SPI_MISO and SPI_MOSI.

I²C timing specifications of table

Parameter	Symbol	Fast-mode Plus ^{a,b}			Unit
		Minimum	Typical	Maximum	
SCL clock frequency	f _{SCL}	0	—	1000	kHz
Bus-free times between a stop and start condition	t _{Buf}	500	—	—	ns
Hold time (repeated) start condition. After this period, the first clock pulse is generated.	t _{HD;STA}	260	—	—	ns
Low period of the SCL clock	t _{LOW}	500	—	—	ns
High period of the SCL clock	t _{HIGH}	260	—	—	ns
Set-up time for a repeated start condition	t _{SU;STA}	260	—	—	ns
Data hold time	t _{HD;DAT}	0 ^c	—	450 ^d	ns
Data setup time	t _{SU;DAT}	260 ^e	—	—	ns
Setup time for stop condition	t _{SU;STO}	260	—	—	ns
Pulse width of spikes suppressed by the input filter	t _{SP}	0	—	10	ns

a. All timing values are referenced to minimum (VIH) and maximum (VIL) levels and were obtained over process, voltage, and temperature.

b. For Fast-mode Plus, the hardware currently supports the 4th mode, not the 3rd mode.

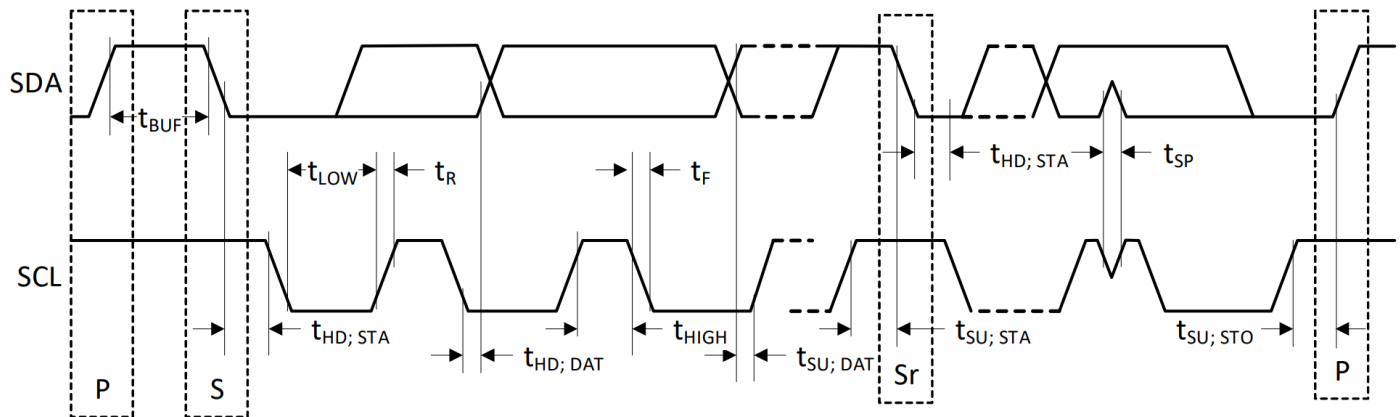
c. A device must internally provide a hold time of at least 300 ns for the serial data (SDA) signal to bridge

the undefined region of the serial clock line (SCL).

d. This must be met because the AP6208 module does not stretch the low period of the SCL signal.

e. A Fast-mode Plus device can be used in Fast mode or Standard mode, but the $TSU, DAT > 100$ ns (Fast mode) or $TSU, DAT > 250$ ns (Standard mode) requirement must be met. This automatically applies because the AP6208 module does not stretch the low period of the SCL signal for Fast-mode Plus.

The below figure shows clock and data timing



The SDA and SCL lines can source and sink 2 mA and have internal 45 k Ω pull-up resistors. To drive the capacitive load of the I2C interface, external pull-up resistors will be required to keep the rise time less than 300 ns between 30% of VDD_IO and 70% of VDD_IO. The rise time is modeled by a simple RC circuit where R is the total pull-up resistance (the parallel combination of the internal and external resistors) and C is the total capacitance of the signal line, the trace capacitance, and all connected pins.

5. RF Specification

5.1 Bluetooth Specification

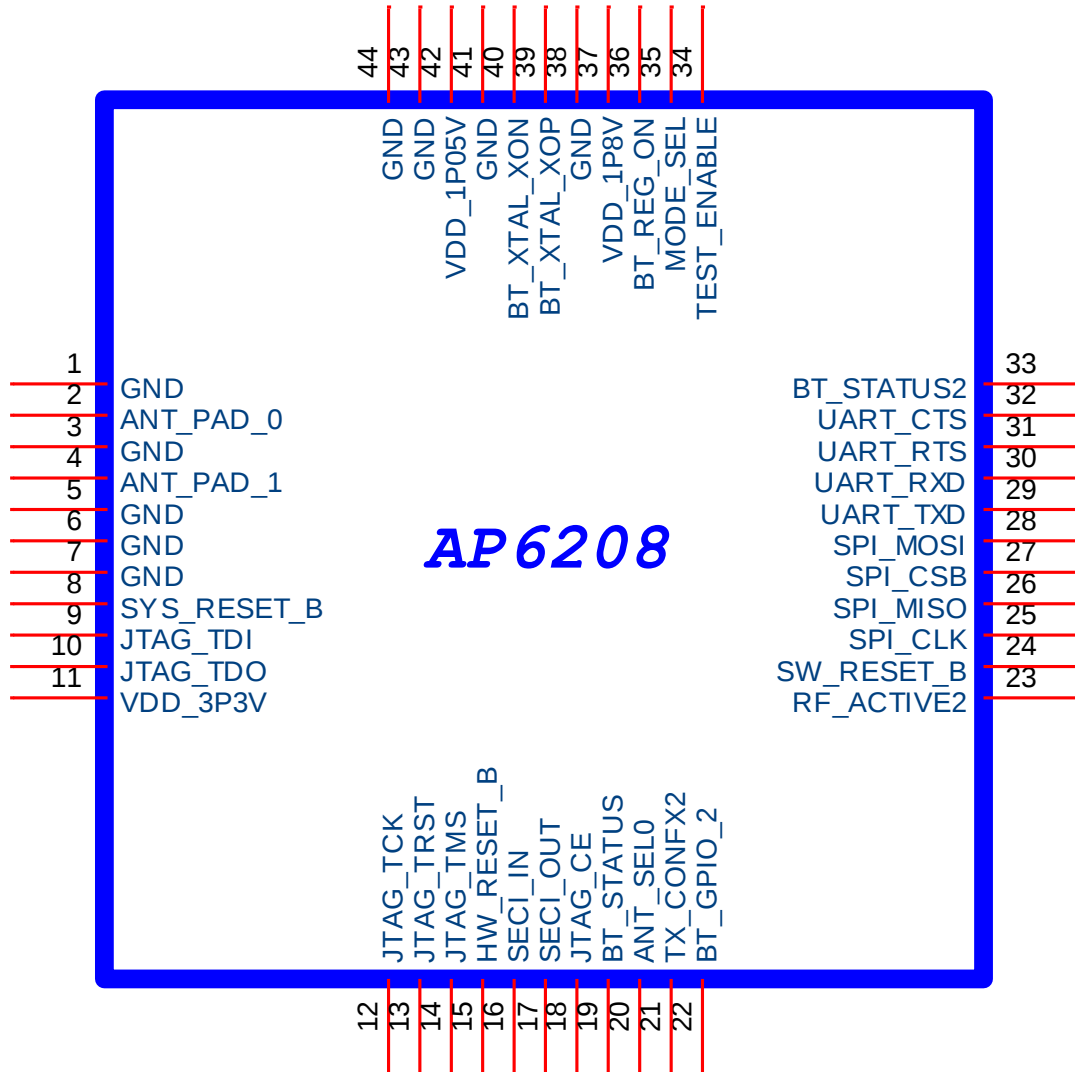
Feature	Description
General Specification	
Bluetooth Standard	BDR、EDR、LE(1Mbps、2Mbps、500 kbps, and 125 kbps)
Frequency Band	2402 MHz ~ 2480 MHz
Number of Channels	40 channels for BLE
Modulation	GFSK, $\pi/4$ -DQPSK
RF Specification	
Output Power, tolerance ± 2.5dB	
	CL1 (dBm)
BDR Output Power	7
EDR Output Power	7
BLE Output Power	7
Sensitivity, tolerance ± 2.5dB	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-90 dBm
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)	-93 dBm
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-87 dBm
Sensitivity @ PER=30.8% for LE (2Mbps)	-92 dBm
Sensitivity @ PER=30.8% for LE (1Mbps)	-94 dBm
Sensitivity @ PER=30.8% for LE (500Kbps)	-101 dBm
Sensitivity @ PER=30.8% for LE (125Kbps)	-105 dBm
Maximum Input Level	GFSK (1Mbps):-20dBm
	$\pi/4$ -DQPSK (2Mbps) :-20dBm

5.2 IEEE 802.15.4 (Thread, Zigbee)(TBD)

IEEE802.15.4 (250Kbps) RF_TX PERFORMANCE					
Item	Sym.	TYP	tolerance		UNIT
Output power		TBD	± 1		dBm
IEEE802.15.4 (250Kbps) RF_RX PERFORMANCE					
Item	Sym.	TYP	tolerance		UNIT
Sensitivity	250Kbps	TBD	± 1		dBm
Frequency Offset					KHz

6. Pinout Information

6.1 Schematic Symbol



6.2 Module Pin Descriptions

The below table provides the signal name, type, and description of each pin in the AP6208 module. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output), if any.

No	Name	Type	Description
1	GND	GND	Ground
2	ANT_PAD_0	I/O	Antenna-0 Dual radio receiver input and transmitter output
3	GND	GND	Ground
4	ANT_PAD_1	I/O	Antenna-1 Dual radio receiver input and transmitter output
5	GND	GND	Ground
6	GND	GND	Ground
7	GND	GND	Ground
8	SYS_RESET_B	I	Miscellaneous Signals External active-low system reset
9	JTAG_TDI	I	Miscellaneous Signals JTAG TDI signal
10	JTAG_TDO	O	Miscellaneous Signals JTAG TDO signal
11	VDD_3P3V	I	3.3V input supply pin for digital padding
12	JTAG_TCK	I	Miscellaneous Signals JTAG TCK signal
13	JTAG_TRST	I	Miscellaneous Signals JTAG Test reset
14	JTAG_TMS	I	Miscellaneous Signals JTAG TMS signal
15	HW_RESET_B	I	Miscellaneous Signals External active-low hardware reset. Warm reset that triggers a FW download.
16	SECI_IN	I	Coexistence Interface SECI_IN when used with another Ampak wireless device; otherwise, TX confirmation (TX_CONFX) input of a primary 3-wire Bluetooth coexistence interface.

17	SECI_OUT	O	Coexistence Interface SECI_OUT when used with another Ampak wireless device; otherwise, RF active (RF_ACTIVE) output of a primary 3-wire Bluetooth coexistence interface.
18	JTAG_CE	I	Miscellaneous Signals JTAG chip-enable input
19	BT_STATUS	O	Miscellaneous Signals STATUS output line of a primary 3-wire Bluetooth coexistence interface
20	ANT_SELO	O	BT_DEV_WAKE HOST Wake-Up Bluetooth Device
21	TX_CONFX2	I	Miscellaneous Signals Usable as the PUART RXD signal. Also usable as the TX confirmation (TX_CONFX) input of a secondary 3-wire Bluetooth coexistence interface.
22	BT_GPIO_2	I/O	Miscellaneous Signals GPIO_2. Usable as an external interrupt source.
23	RF_ACTIVE2	O	(1)Miscellaneous Signals RF_ACTIVE output line of a secondary 3-wire Bluetooth coexistence interface or usable as a debugging port (2)BT_HOST_WAKE Bluetooth Device to Wake-Up HOST
24	SW_RESET_B	I	Miscellaneous Signals External active-low software reset. Warm reset that does not trigger a FW download.
25	SPI_CLK	O	Serial Peripheral Interface SPI clock
26	SPI_MISO	I	Serial Peripheral Interface SPI main in, subnode out
27	SPI_CSB	O	Serial Peripheral Interface SPI chip select
28	SPI_MOSI	O	Serial Peripheral Interface SPI main out, subnode in
29	UART_TXD	O	UART Interface UART serial output.

30	UART_RXD	I	UART Interface UART serial input.
31	UART_RTS	O	UART Interface UART request-to-send.
32	UART_CTS	I	UART Interface UART clear-to-send.
33	BT_STATUS2	O	Miscellaneous Signals Usable as the PUART TXD signal. Also usable as the STATUS output line of a secondary 3-wire Bluetooth coexistence interface.
34	TEST_ENABLE	I	Miscellaneous Signals 0: Normal operating mode 1: Test mode.
35	MODE_SEL	I	Miscellaneous Signals Mode selection: 0: MCM mode 1: Standalone mode
36	BT_REG_ON	I	Miscellaneous Signals 0: Turn internal PMU off. 1: Turn internal PMU on.
37	VDD_1P8V	I	1.8V VDDIO input supply pin
38	GND	GND	Ground
39	BT_XTAL_XOP	I	Crystal (XTAL) Interface External 80MHz_XTAL oscillator input
40	BT_XTAL_XON	O	Crystal (XTAL) Interface External 80MHz_XTAL oscillator output
41	GND	GND	Ground
42	VDD_1P05V	I	1.05V input supply pin for radio circuit
43	GND	GND	Ground
44	GND	GND	Ground

Notes:

This is original define. More Alternate function mapping reference to below table

6.3 GPIO Alternative Signal Functions

GPIO stands for general purpose input/output. It is a type of pin found on an integrated circuit that does not have a specific function. While most pins have a dedicated purpose, such as sending a signal to a certain component, the function of a GPIO pin is customizable and can be controlled by the software.

6.3.1 Core-level Mux selection Table

Pin	Function Number											
	0	1	3	4	5	6	7	11	12	13	14	15
BT_UART_CTS_N	UART_CTS_N	—	—	—	UART2_RTS_N	—	A_GPIO[1]	—	—	SPI_CS B	—	—
BT_UART_RTS_N	UART_RTS_N	—	—	—	UART2_CTS_N	—	A_GPIO[0]	—	—	SPI_MISO	—	—
BT_UART_RXD	UART_RXD	—	—	SDA	UART2_RXD	—	GPIO[5]	—	—	SPI_MOSI	—	—
BT_UART_TXD	UART_TXD	—	—	SCL	UART2_TXD	—	GPIO[4]	—	—	SPI_CLOCK	—	—
BT_CORE_SIG_0	A_GPIO[0]	—	—	—	—	—	—	—	—	—	—	SPI_CLOCK
BT_CORE_SIG_1	A_GPIO[1]	—	—	—	—	—	—	—	—	—	—	SPI_CS B
BT_CORE_SIG_2	A_GPIO[2]	—	—	—	—	—	—	—	SDA	—	—	SPI_MOSI
BT_CORE_SIG_3	A_GPIO[3]	—	—	—	—	—	—	—	SCL	—	—	SPI_MISO
BT_CORE_SIG_4	A_GPIO[5]	—	—	—	—	—	—	UART2_RTS_N	SCL	—	—	SPI_MOSI
BT_CORE_SIG_5	A_GPIO[6]	—	—	—	—	—	—	UART2_CTS_N	—	SDA	—	SPI_MISO
BT_CORE_SIG_6	GPIO[7]	—	—	—	—	—	—	UART2_RXD	—	—	—	SPI_CS B
BT_CORE_SIG_7	GPIO[6]	—	—	—	—	—	—	UART2_TXD	—	—	—	SPI_CLOCK
BT_CORE_SIG_8	GPIO[1]	—	—	—	—	—	—	—	—	—	—	—

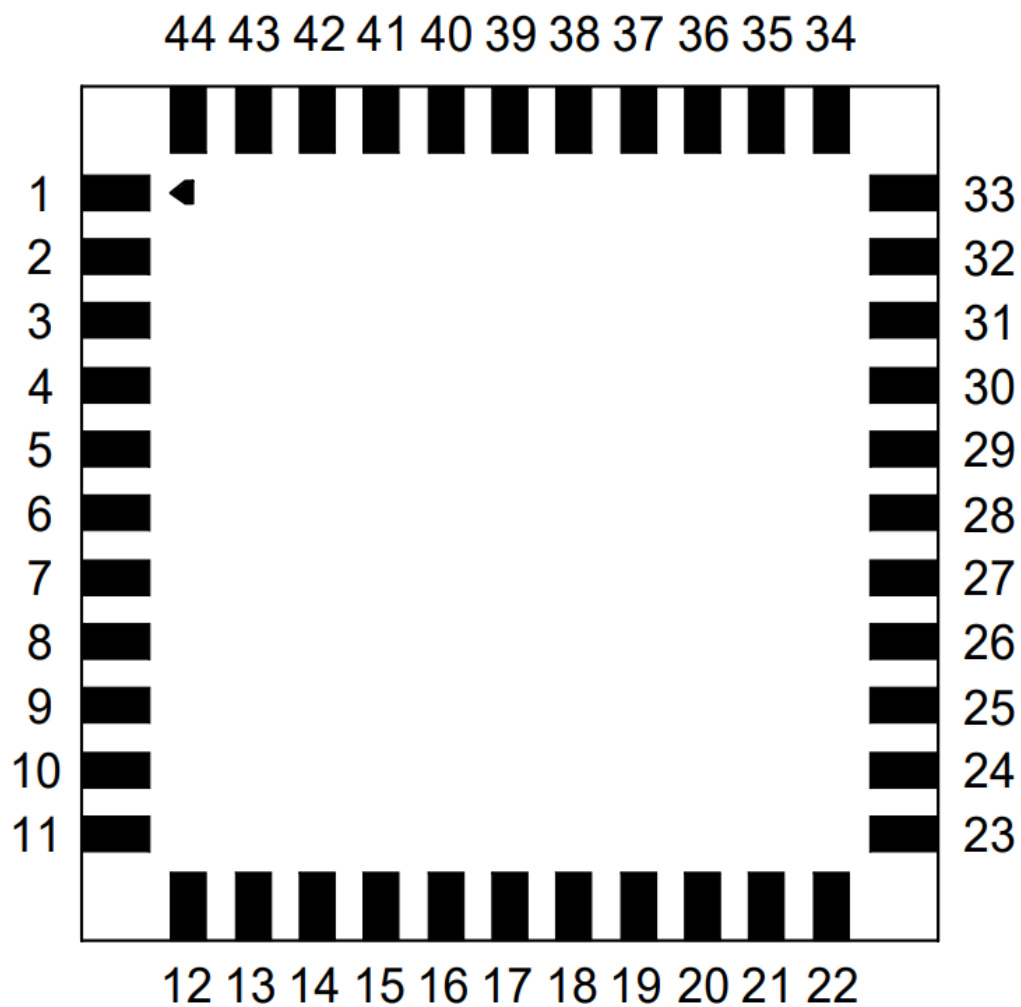
Pin	Function Number											
	0	1	3	4	5	6	7	11	12	13	14	15
BT_CORE_SIG_9	—	—	—	—	—	—	A_GPIO[7]	—	—	—	—	—
BT_CORE_SIG_10	GPIO[0]	—	—	—	—	—	—	—	—	—	—	—
BT_GPIO5	GPIO[5]	—	—	—	—	—	—	UART2_CTS_N	—	—	—	SCL
BT_GPIO4	GPIO[4]	—	—	—	—	—	—	UART2_RTS_N	—	—	—	SDA
BT_GPIO3	GPIO[3]	UART2_TXD	—	—	—	—	—	—	—	—	—	—
BT_GPIO2	GPIO[2]	—	UART2_RTS_N	—	—	—	—	—	—	—	—	—
BT_AJTAG_TDI	AJTAG_TDI	—	—	SPI_MISO	GPIO[5]	GPIO[6]	GPIO[7]	—	A_GPIO[4]	A_GPIO[5]	A_GPIO[6]	SDA
BT_AJTAG_TDO	AJTAG_TDO	—	—	SPI_MOSI	GPIO[5]	GPIO[6]	GPIO[7]	—	A_GPIO[4]	A_GPIO[5]	A_GPIO[6]	SCL
BT_AJTAG_TMS	AJTAG_TMS	—	—	SPI_CSB	GPIO[5]	GPIO[6]	GPIO[7]	—	A_GPIO[4]	A_GPIO[5]	A_GPIO[6]	—
BT_AJTAG_TCK	AJTAG_TCK	—	—	SPI_CLK	GPIO[5]	GPIO[6]	GPIO[7]	—	A_GPIO[4]	A_GPIO[5]	A_GPIO[6]	—

6.3.2 Top-level Mux selection Table

Pad Name	Function Number			
	0 (Default)	1	2	3
TDI	BT_AJTAG_TDI	BT_AJTAG_TDI	BT_AJTAG_TDI	BT_AJTAG_TDI
TDO	BT_AJTAG_TDO	BT_AJTAG_TDO	BT_AJTAG_TDO	BT_AJTAG_TDO
TMS	BT_AJTAG_TMS	BT_AJTAG_TMS	BT_AJTAG_TMS	BT_AJTAG_TMS
TCK	BT_AJTAG_TCK	BT_AJTAG_TCK	BT_AJTAG_TCK	BT_AJTAG_TCK
UART_CTS	BT_UART_CTS_N	BT_UART_CTS_N	BT_UART_CTS_N	BT_UART_CTS_N
UART_RTS	BT_UART_RTS_N	BT_UART_RTS_N	BT_UART_RTS_N	BT_UART_RTS_N
UART_RXD	BT_UART_RXD	BT_UART_RXD	BT_UART_RXD	BT_UART_RXD
UART_TXD	BT_UART_TXD	BT_UART_TXD	BT_UART_TXD	BT_UART_TXD
SPI_CLK	BT_CORE_SIG_0	BT_CORE_SIG_0	BT_CORE_SIG_0	BT_CORE_SIG_0
SPI_CSB	BT_CORE_SIG_1	BT_CORE_SIG_1	BT_CORE_SIG_1	BT_CORE_SIG_1
SPI_MISO	BT_CORE_SIG_2	BT_CORE_SIG_2	BT_CORE_SIG_2	BT_CORE_SIG_2
SPI_MOSI	BT_CORE_SIG_3	BT_CORE_SIG_3	BT_CORE_SIG_3	BT_CORE_SIG_3
SECI_IN	SECI_IN	—	TX_CONFX	—
SECI_OUT	SECI_OUT	—	RF_ACTIVE	—
BT_STATUS	BT_CORE_SIG_9	—	—	BT_STATUS
TX_CONFX2	BT_CORE_SIG_6	—	—	TX_CONFX2
RF_ACTIVE 2	BT_CORE_SIG_8	—	—	RF_ACTIVE2
BT_STATUS 2	BT_CORE_SIG_7	—	—	BT_STATUS2
ANT_SELO	ANT_SELO	BT_CORE_SIG_10	—	—

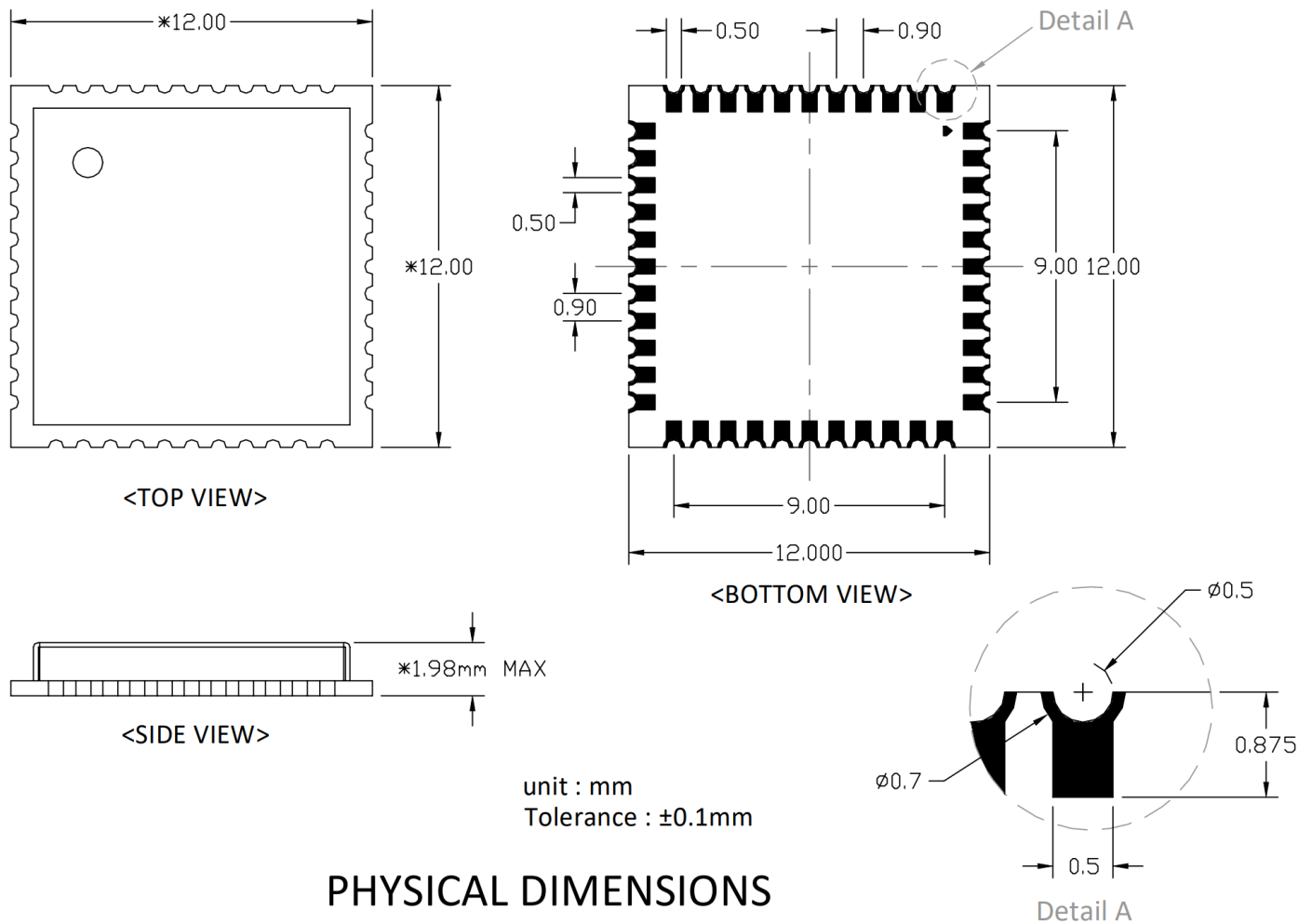
6.4 Module Pin Number Define

PIN OUTLINE <TOP VIEW>



7. Dimensions

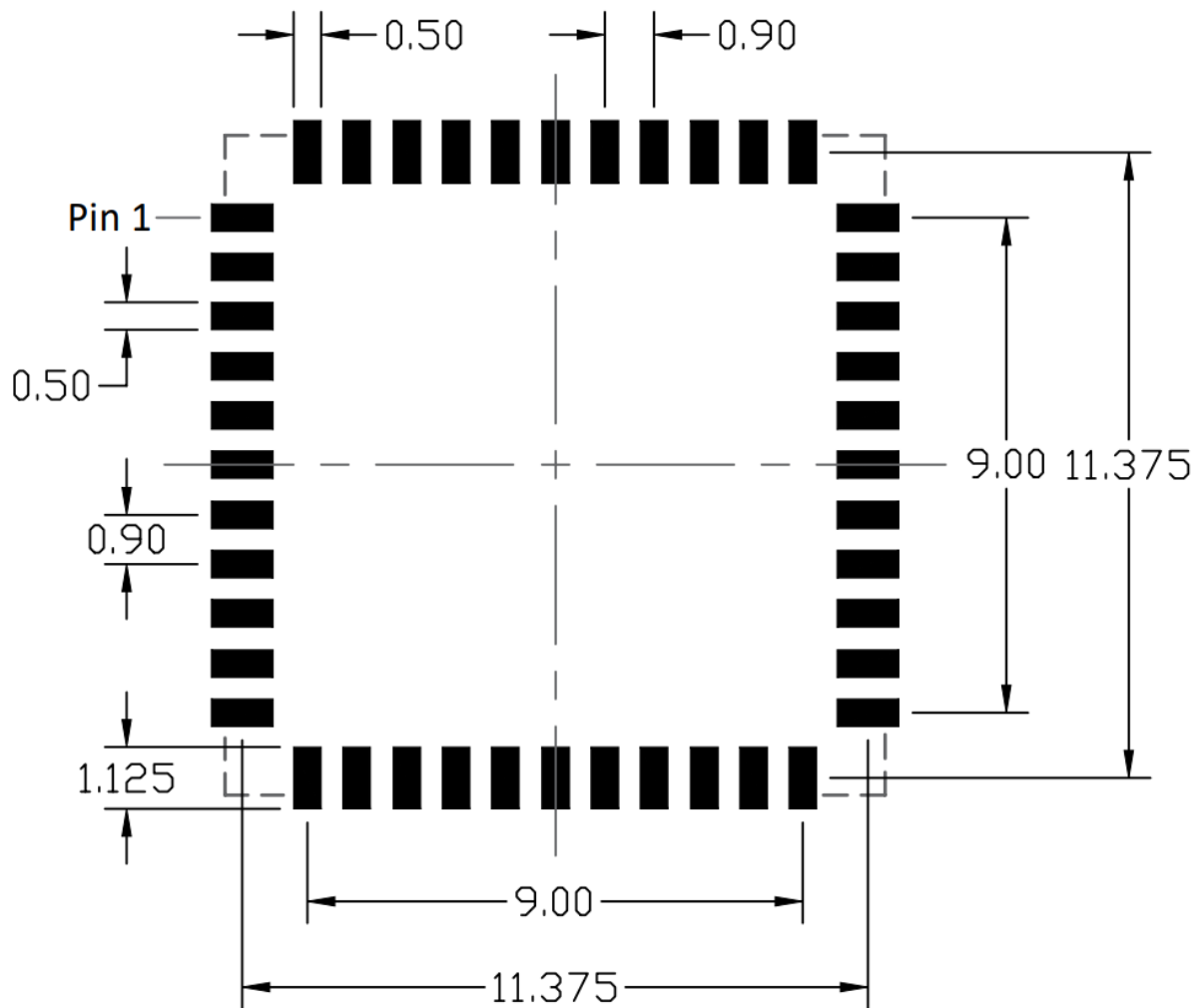
7.1 Module Physical Dimension



7.2 Module Recommended Footprint

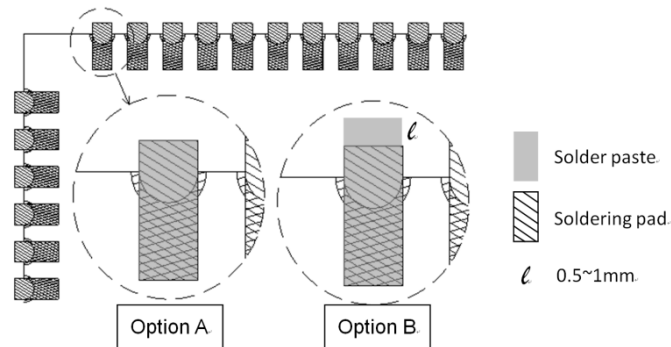
RECOMMENDED FOOTPRINT

<TOP VIEW>

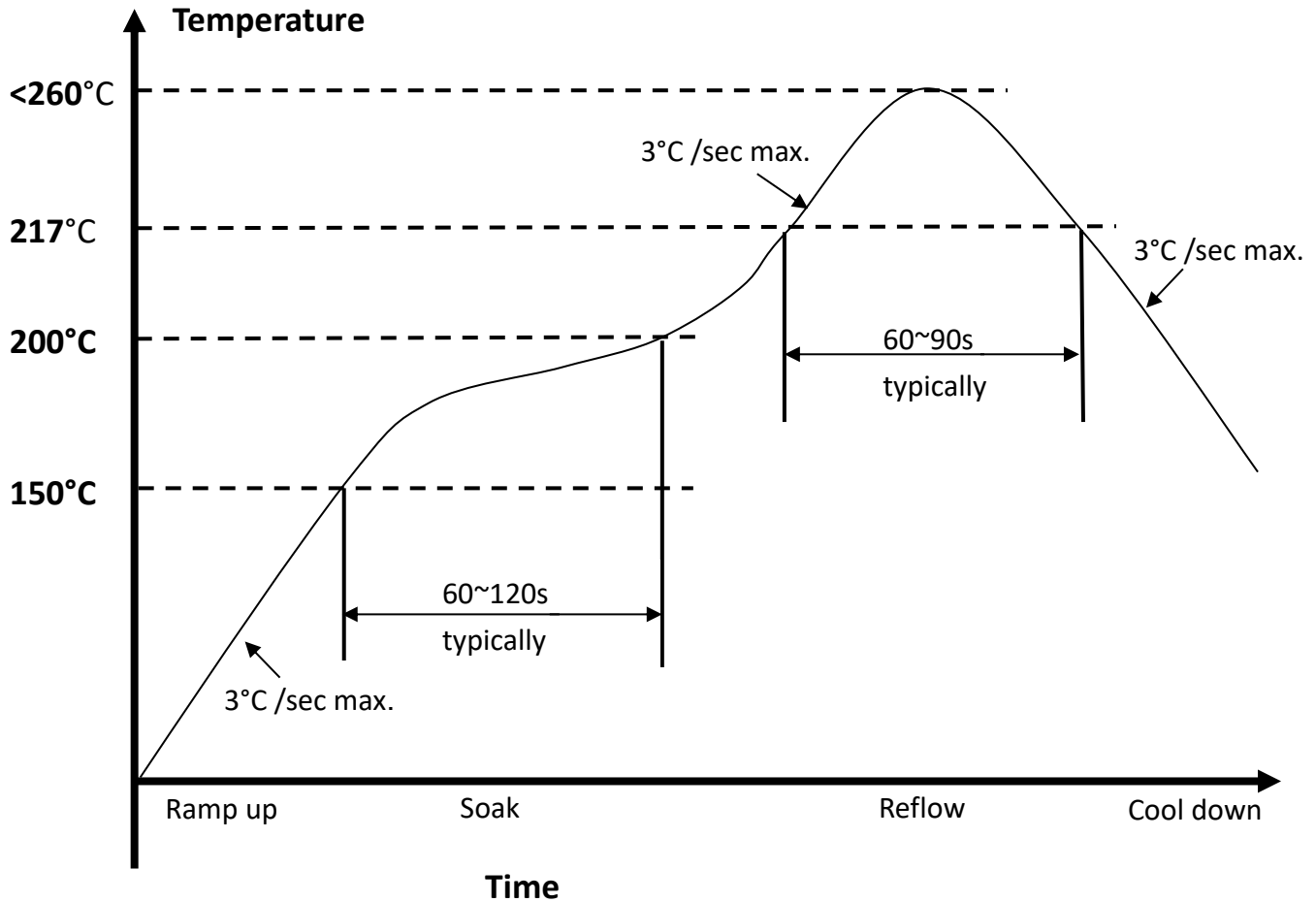


Unit : mm

- Solder paste layer design is generally the same as recommended footprint.
(錫膏層設計通常建議和焊墊尺寸相同)
- If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial.
In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact AMPAK FAE for assistance.
(如果模組吃錫品質考量側面爬錫，如何優化鋼網開孔設計以調整適當的錫膏量是非常重要的。尤其鋼網的厚度大約是 0.1mm 或更薄時，可考慮局部加厚鋼網的設計。請諮詢製程工程師以優化鋼網的設計,或是聯絡正基科技技術支持團隊).



8. Recommended Reflow Profile

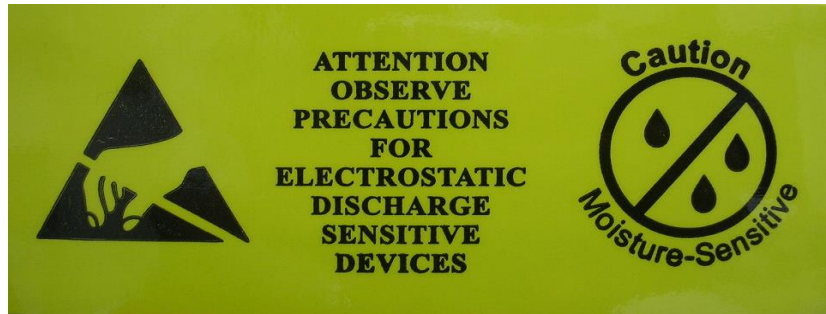


1. Referred to IPC/JEDEC standard
2. Peak Temperature : <260°C (Time within 5°C of actual Peak Temperature 20-40 seconds)
3. Cycle of Reflow : 2 times max.
4. Adding Nitrogen (N₂) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component

9. Package Information

9.1 Label

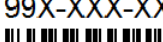
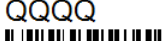
Label A → Anti-static and humidity notice



Label B → MSL caution / Storage Condition

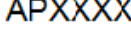
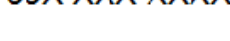
	Caution This bag contains MOISTURE-SENSITIVE DEVICES	LEVEL 
		If blank, see adjacent bar code label
1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH) 2. Peak package body temperature: _____ °C If blank, see adjacent bar code label 3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be a) Mounted within: _____ hours of factory conditions If blank, see adjacent bar code label ≤30°C/60% RH, or b) Stored per J-STD-033 4. Devices require bake, before mounting, if: a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C b) 3a or 3b are not met 5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure Bag Seal Date: _____ If blank, see adjacent bar code label Note: Level and body temperature defined by IPC/JEDEC J-STD-020		

Label C → Inner box label .

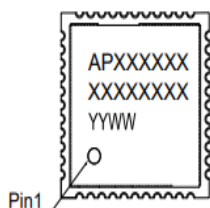
PO:	 -
AMK DEVICE:	 -
PKG S/N:	 9PKGYYMMDDNNNNN
Model Name:	 APXXXXXXXXX (R3HF)
P/N:	 99X-XXX-XXXXR
Quantity:	 QQQQ
Date Code:	 YYWW
Lot Code:	 XXXXXXXXXX

Label D → Carton box label .

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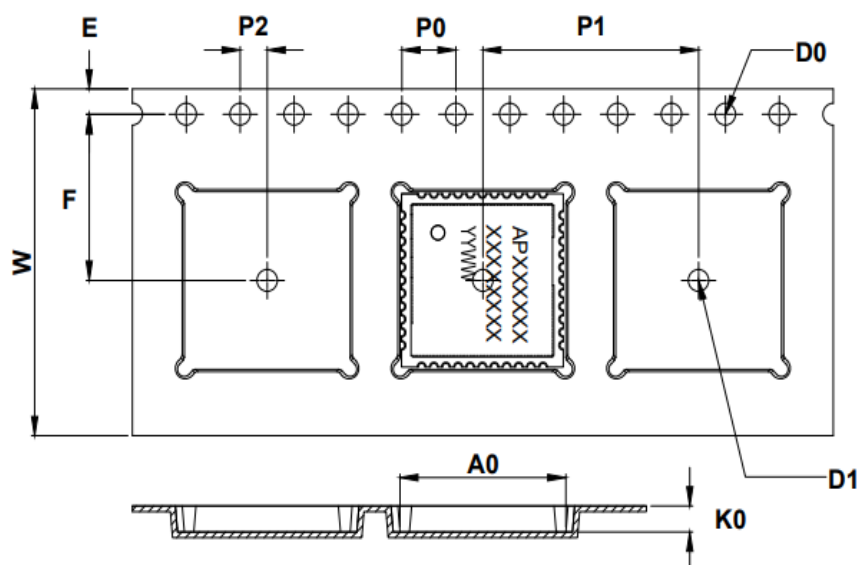
PO:	 -
AMK DEVICE:	 -
Model Name:	 APXXXXXXXXX (R3HF)
Part No.:	 99X-XXX-XXXXR
Quantity:	 QQQQ
Lot D/C:	 XXXXXXXXXX YYWW QQQQ
Manufacture:	 YYYY/MM/DD

9.2 Label Packing Dimension



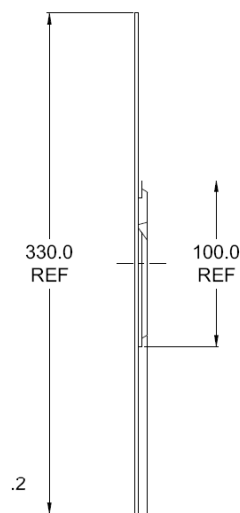
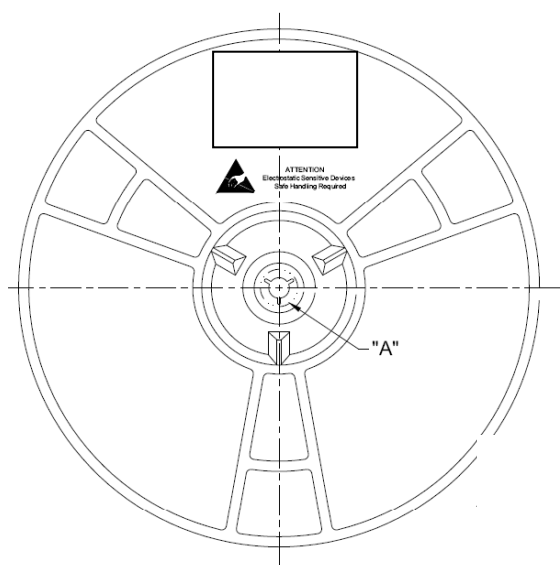
Rows	Content	Note
Row 1	APXXXXXX	Model Name
Row 2	XXXXXXXX or XXXXXXXXX (8 digitals or 9 digitals)	Lot Code
Row 3	YYWW	Date Code
Row 4	Through hole or non through hole	Pin1

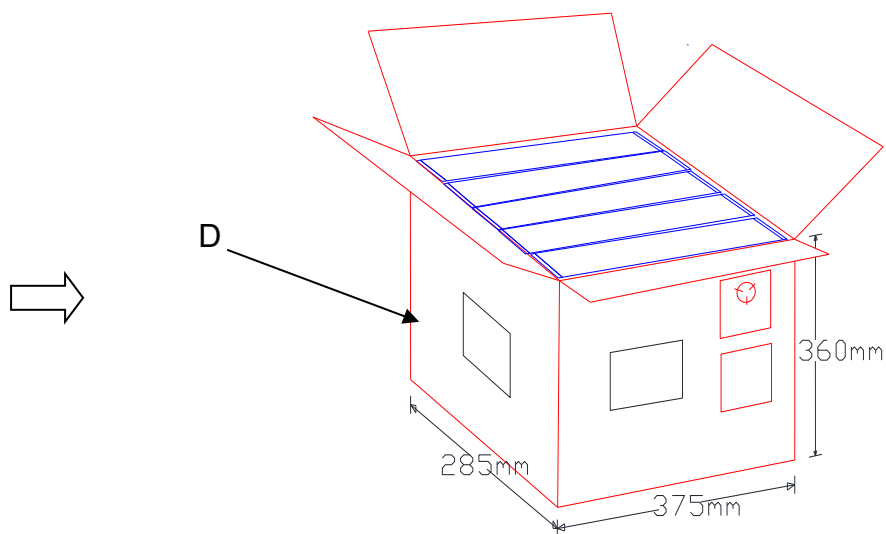
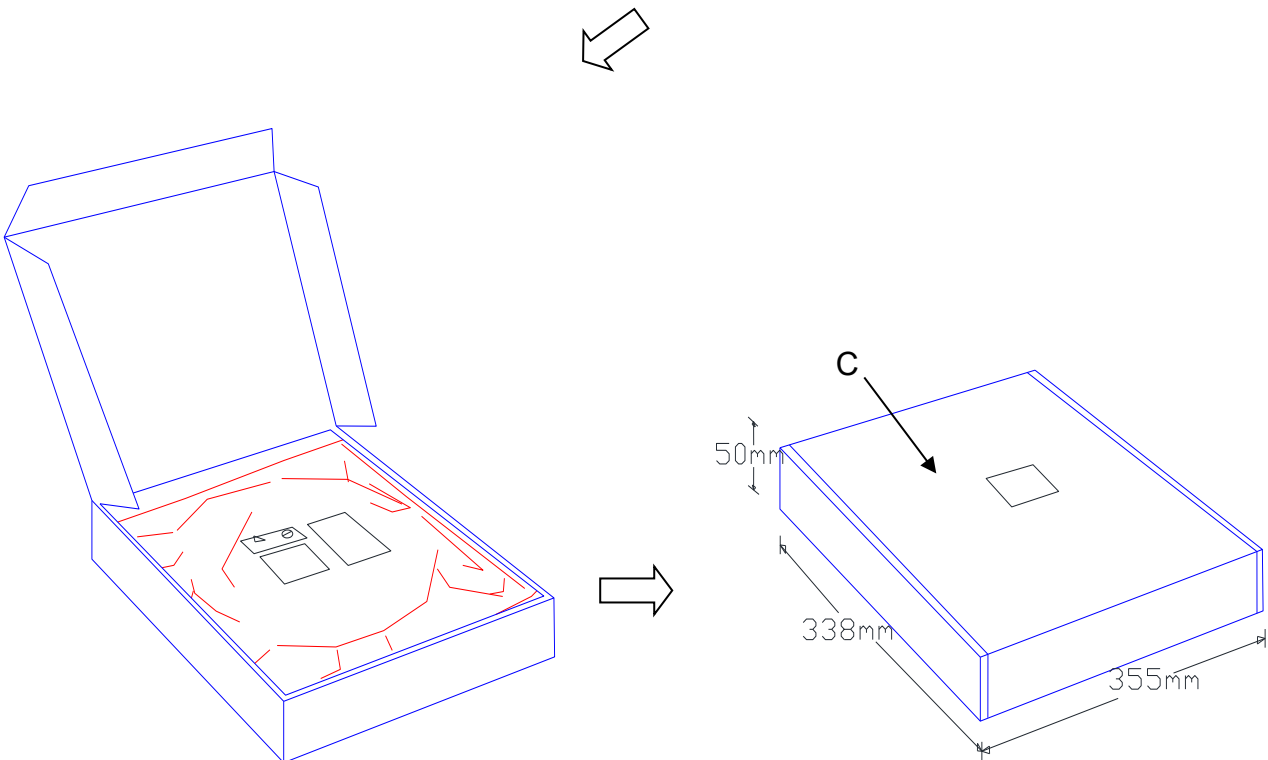
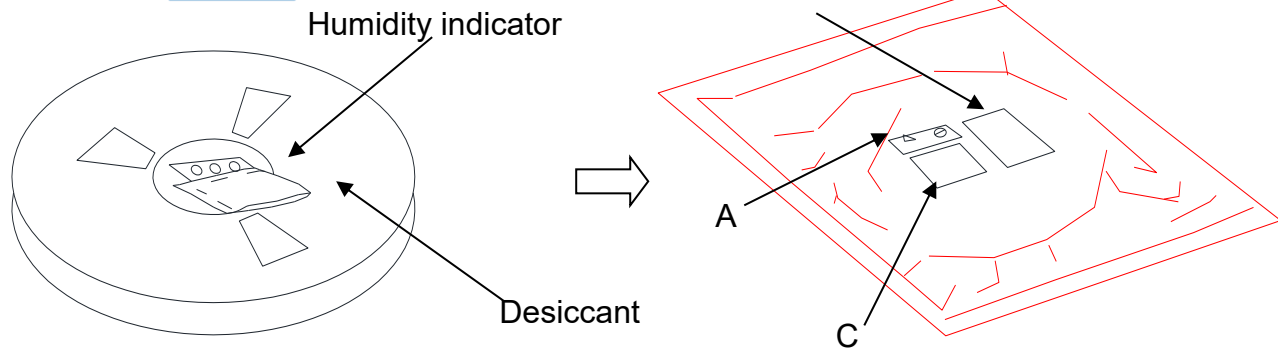
Packaging Type	Packing Quantity	Note
Reel / Bag / Box	1500pcs	13" reel
Carton	7500pcs	5Box



W	24.00±0.30
A0	12.30±0.10
B0	12.30±0.10
K0	1.80±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	16.00±0.10
P2	2.00±0.10
D0	1.50 ^{+0.10} _{-0.00}
D1	φ1.50MIN

1. Material : Black Conductive Polystyrene Alloy.
2. All dimensions meet EIA-481-D requirements.
3. Thickness : 0.30±0.05mm.





9.3 MSL Level / Storage Condition

	Caution This bag contains MOISTURE-SENSITIVE DEVICES	LEVEL 4 If blank, see adjacent bar code label
1. Calculated shelf life in sealed bag: 12 months at $<40^{\circ}\text{C}$ and $<90\%$ relative humidity (RH) 2. Peak package body temperature: <u>250</u> $^{\circ}\text{C}$ If blank, see adjacent bar code label 3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be a) Mounted within: <u>72</u> hours of factory conditions If blank, see adjacent bar code label $\leq 30^{\circ}\text{C} / 60\% \text{ RH, or}$ b) Stored per J-STD-033 4. Devices require bake, before mounting, if: a) Humidity Indicator Card reads $>10\%$ for level 2a-5a devices or $>60\%$ for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$ b) 3a or 3b are not met. 5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure. Bag Seal Date: _____ If blank, see adjacent bar code label Note: Level and body temperature defined by IPC/JEDEC J-STD-020		

10. Order Information

Item	Product Name	Description
1	AP6208	2.4 GHz, Dual-Radio Bluetooth 5.4 and IEEE 802.15.4 Module & Board I/O ANT_PAD